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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,494	04/07/2004	Kishor V. Desai	03-2198/LSI1P242	7404
24319	7590	07/13/2005	EXAMINER	
LSI LOGIC CORPORATION			SEFER, AHMED N	
1621 BARBER LANE				
MS: D-106			ART UNIT	PAPER NUMBER
MILPITAS, CA 95035			2826	

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/820,494	DESAI ET AL.
Examiner	Art Unit	
A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 19 May 2005.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-28 is/are pending in the application.  
4a) Of the above claim(s) 15-28 is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-14 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on \_\_\_\_\_ is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All    b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

• Attachment(s)

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .

5)  Notice of Informal Patent Application (PTO-152)

6)  Other: \_\_\_\_ .

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I (claims 1-14) in the reply filed on 5/19/2005 is acknowledged.

### *Specification*

2. The disclosure is objected to because of the following informalities: In par. 0027, "a first layer 201" and "a second layer 203" should read "a first layer 202" and "a second layer 204" respectively. Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Bunyan ("Bunyan") USPN 6,432,497.

Bunyan discloses in fig. 1 a semiconductor package comprising: a packaging substrate 14; a semiconductor die 12 mounted with the substrate; a heatspreader 22 and a multi-layer heat transfer element 23 arranged between the semiconductor die and the heat spreader to enable thermal communication between the die and the heat spreader.

Regarding claim 2, Bunyan discloses a core spacer element 30 having a top surface and a bottom surface; a first layer 20 of thermally conductive reflowable material formed on the top surface; and a second layer 18 of thermally conductive reflowable material formed on the bottom surface.

Regarding claim 3, Bunyan discloses the die 12 being attached to the second layer 18 and wherein the heat spreader 22 is attached to the first layer 20.

As to the reflow process recited in the claim, it refers to a process and "product by process" claims are directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685 and *In re Thorpe*, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

Regarding claim 4, Bunyan discloses (paragraph bridging cols. 9 and 10) the core spacer element 30 being comprised of conducting materials.

Regarding claim 9, Bunyan discloses (col. 10, lines 60-67) the core spacer element 30 being comprised of conducting resin material.

5. Claims 1, 2, 4, 5, 7, 8, 10 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. ("Chen") USPN 6,716,676.

Chen discloses in fig. 7 a semiconductor package comprising: a packaging substrate 300; a semiconductor die 320 mounted with the substrate; a heatspreader 370 and a multi-layer heat transfer element (321, 332, 321/375) arranged between the semiconductor die and the heat spreader to enable thermal communication between the die and the heat spreader.

Regarding claim 2, Chen discloses a core spacer element 332 having a top surface and a bottom surface; a first layer 321/375 of thermally conductive reflowable material formed on the top surface; and a second layer 321 of thermally conductive reflowable material formed on the bottom surface.

Regarding claims 4 and 5, Chen discloses the core spacer element 332 being comprised of conducting materials or metal (as in claim 5).

Regarding claims 7 and 8, Chen discloses in fig. 3B vias 333 that penetrate through the core spacer element or dimples formed therein (as in claim 8).

Regarding claim 10, Chen discloses the first layer and the second layer each comprising solder materials.

Regarding claim 11, Chen discloses the semiconductor die being mounted to the packaging substrate using a plurality of solder bumps 311; wherein the packaging substrate includes a stiffener 350 element that is mounted between the heat spreader and the substrate.

6. Claims 1-10, 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Karnezos (“Karnezos”) USPN 6,906,416.

Karnezos discloses in fig. 5 a semiconductor package comprising: a packaging substrate; a semiconductor die 414/514 mounted with the substrate; a heatspreader 530 and a multi-layer heat transfer element (521, 512, 523) arranged between the semiconductor die and the heat spreader to enable thermal communication between the die and the heat spreader.

Regarding claim 2, Karnezos discloses a core spacer element 512 having a top surface and a bottom surface; a first layer 523 of thermally conductive reflowable material formed on the

top surface; and a second layer 521 of thermally conductive reflowable material formed on the bottom surface.

Regarding claim 3, Karnezos discloses the die 514 being attached to the second layer 521 and wherein the heat spreader 530 is attached to the first layer 523.

As to the reflow process recited in the claim, it refers to a process and "product by process" claims are directed to the product *per se*, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685 and *In re Thorpe*, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

Regarding claims 4-6 and 9, Karnezos discloses (col. 16, lines 13-38) the core spacer element 512 being comprised of conducting materials or metal (as in claim 5) or layers of metal (as in claim 6) or conducting resin material (as in claim 9).

Regarding claims 7 and 8, Karnezos discloses vias 522 that penetrate through the core spacer element or dimples formed therein (as in claim 8).

Regarding claim 10, Karnezos discloses the first layer and the second layer each comprising solder materials.

Regarding claim 12, Karnezos discloses the first layer being formed of a solder material that has good adhesion to a material comprising a surface of the heat spreader; and wherein the second layer being formed of a solder material that has good adhesion to a material comprising a top surface of the die.

Regarding claim 13, Karnezos discloses (col. 16, lines 13-38) core spacer 512 comprising a thermally non-conductive material and wherein the core spacer element includes a plurality of vias 522 that penetrate through the core spacer element; wherein reflowable material of at least one of the first material and the second material fills at least a portion of the vias so that said first layer and second layer are in physical contact with each other, thereby establishing thermal communication between the die and the heat spreader.

7. Claims 1-3 and 10-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Oman (“Oman”) USPN 6,873,043.

Oman discloses in figs. 1 and 2 a semiconductor package comprising: a packaging substrate 14; a semiconductor die 12 mounted with the substrate; a heatspreader 26 and a multi-layer heat transfer element 32 arranged between the semiconductor die and the heat spreader to enable thermal communication between the die and the heat spreader.

Regarding claim 2, Oman discloses a core spacer element 36 having a top surface and a bottom surface; a first layer 38 of thermally conductive reflowable material formed on the top surface; and a second layer 34 of thermally conductive reflowable material formed on the bottom surface.

Regarding claim 3, Oman discloses the die 12 being attached to the second layer 34 and wherein the heat spreader 26 being attached to the first layer 38.

As to the reflow process recited in the claim, it refers to a process and "product by process" claims are directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685 and *In re Thorpe*, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long

as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

Regarding claim 10, Oman discloses (col. 4, lines 15-20) the first layer and the second layer each comprise solder materials.

Regarding claim 11, Oman discloses the semiconductor die being mounted to the packaging substrate using a plurality of solder bumps (col. 5, lines 15-17); wherein the packaging substrate includes a stiffener 44/46 element that is mounted between the heat spreader and the substrate.

Regarding claim 12, Oman discloses the first layer being formed of a solder material that has good adhesion to a material comprising a surface of the heat spreader; and wherein the second layer being formed of a solder material that has good adhesion to a material comprising a top surface of the die.

8. Claims 1-6, 10, 12 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Dyckman et al. ("Dyckman") USPN 6,657,864.

Dyckman discloses in fig. 1 a semiconductor package comprising: a packaging substrate 30; a semiconductor die 20 mounted with the substrate; a heatspreader 70 and a multi-layer heat transfer element (62, 50, 63) arranged between the semiconductor die and the heat spreader to enable thermal communication between the die and the heat spreader.

Regarding claim 2, Dyckman discloses a core spacer element 50 having a top surface and a bottom surface; a first layer 63 of thermally conductive reflowable material formed on the top surface; and a second layer 62 of thermally conductive reflowable material formed on the bottom surface.

Regarding claim 3, Dyckman discloses the die 20 being attached to the second layer 62 and wherein the heat spreader 70 being attached to the first layer 63.

As to the reflow process recited in the claim, it refers to a process and "product by process" claims are directed to the product *per se*, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685 and *In re Thorpe*, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

Regarding claims 4-6, Dyckman discloses the core spacer element 50 being comprised of conducting materials or metal (as in claim 5) or layers of metal -- thin and thick portions of layer 50 -- (as in claim 6).

Regarding claim 10, Dyckman discloses the first layer and the second layer each comprise solder materials.

Regarding claim 12, Dyckman discloses the first layer being formed of a solder material that has good adhesion to a material comprising a surface of the heat spreader; and wherein the second layer being formed of a solder material that has good adhesion to a material comprising a top surface of the die.

Regarding claim 14, Dyckman discloses the backside of the packaging substrate has a plurality of solder balls 35 configured for attaching and electrically connecting the package with a circuit board 40; and the heat spreader being attached the first layer, the die being attached to the second layer, solder balls of the substrate being attached the circuit board.

As to the reflow process recited in the claim, it refers to a process and "product by process" claims are directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685 and *In re Thorpe*, 227 USPQ 964, 966. Therefore, the way the product was made does not carry any patentable weight as long as the claims are directed to a device. Further, note that the applicant has the burden of proof in such cases, as the above case law makes clear. Also see MPEP 2113.

  
NATHAN J. FLYNN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS  
July 7, 2005